Study, Characterization, and application of SOI FinFET Transistors on OTA circuit.

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***Abstract*—This paper presents the study, characterization, and application of SOI FinFET transistors in a basic analog block. The analysis of SOI FinFET performance was based on its experimental measurements for different fin widths (W_{Fin}). The analyzed parameters were threshold voltage, subthreshold slope, transconductance, output conductance, Early voltage, and intrinsic voltage gain. The reduction of W_{Fin} resulted in a considerable improvement in all parameters due to the greater electrostatic coupling between the gates and channel. Based on the characterization results, the SOI FinFET with W_{Fin}=20nm was modeled in the HSpice software for its application on a two-stage operational transconductance amplifier (OTA). The proposed OTA achieved a voltage gain of 68dB and a unit gain frequency of 2GHz, demonstrating the great analog potential of these transistors.**

Keywords—SOI FinFET, Silicon-On-Insulator, two-stage amplifier, analog circuit with SOI FinFETs.

I. Introduction

With technological evolution and the consequent reduction in device dimensions, MOS technology for manufacturing digital integrated circuits in ultra-large-scale integration (ULSI) has become increasingly complex.

The SOI (Silicon on Insulator) technology [1-5] then emerged as an alternative to conventional MOS technology, as the devices are manufactured in a silicon layer over an insulator, typically SiO_2, separating the active part of the transistor from the rest of the substrate. This results in lower parasitic capacitance, suppression of the parasitic thyristor effect, and better dielectric isolation between the devices.

SOI technology, however, also begins to present issues with charge control in the channel region for transistors with a channel length below 22nm. One of the solutions found to improve the control of these charges in the channel region is the use of SOI multi-gate transistors with vertical channels, also known as 3D transistors or FinFETs [1,5].

This thin-fin-based geometry presents a significant improvement in transistor performance compared to its planar configuration, such as better electrostatic coupling, which results in lower susceptibility to short-channel effects and higher drain current [1].

In this work the FinFET technology is analyzed through its electrical parameters such as threshold voltage, subthreshold slope, transconductance, output conductance, Early voltage, and intrinsic voltage gain, as well as its application in one analog circuits by simulating a two-stage amplifier circuit with SOI FinFETs.

The amplifier was simulated using HSpice software, and the FinFETs were modeled based on its experimental behavior.

II. Materials and Methods

The studied devices in this work were fabricated at IMEC (Leuven, Belgium). The specifications of the measured devices are presented in Table 1.

Table 1. Specifications of the measured devices.

Parameter	Value
Fin height (H_{Fin})	65 nm
Gate oxide composition	2nm HfSiON + 1nm SiO_2
Equivalent oxide thickness (EOT)	2nm
Buried oxide thickness (t_{BOX})	145nm
Gate electrode composition	10nm TiN + 100nm Polycrystalline silicon
Channel doping (N_A)	10^{15} cm^{-3}

The studied device has a channel length of L_{eff}=150 nm and a fin width varied from 870 nm down to 20 nm. The software used for the amplifier simulation is HSpice.

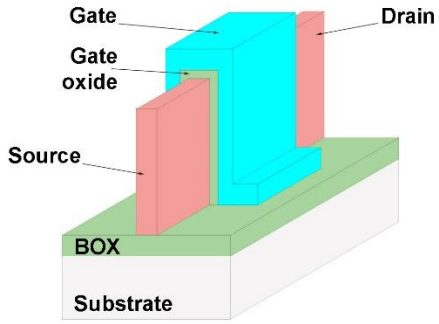
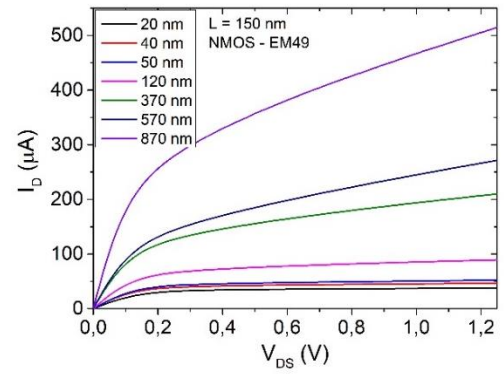


Figure 1. Schematic structure of multi-gate SOI FinFET transistors.

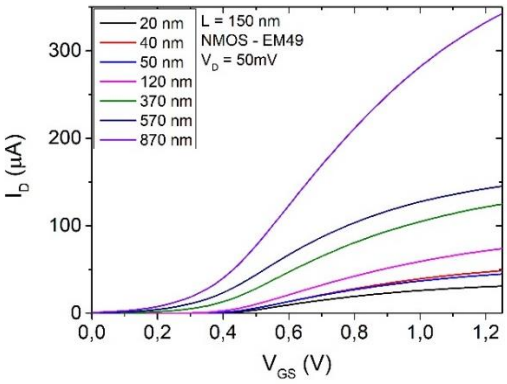
III. Results

Based on the measurements obtained from two cascades of transistors (nMOS and pMOS) with different fin widths, the I_DxV_{GS} and I_DxV_{DS} curves, and the parameters V_{Th}, SS, DIBL, V_{EA}, and A_V were analyzed.

Figure 2 presents the drain current curves as a function of the drain (A) and gate (B) voltages, showing the dependence of I_D on fin width, where a larger W_{Fin} results in an increase in the total current of the device due to the direct relation between drain current and effective channel width. It is also possible to observe the better behavior of the drain curve in the transistor's saturation region (smaller influence of the channel length modulation) obtained to thinner devices due to the better electrostatic coupling between gates.

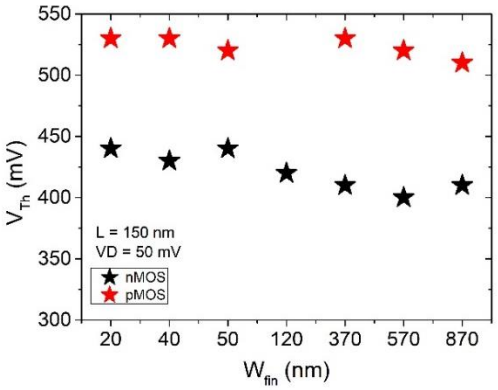


(A)

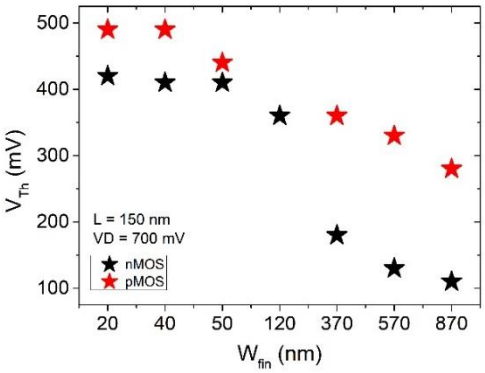


(B)

Figure 2. Experimental I_DV_{DS} (A) and I_DV_{GS} (B) curves.



(A)



(B)

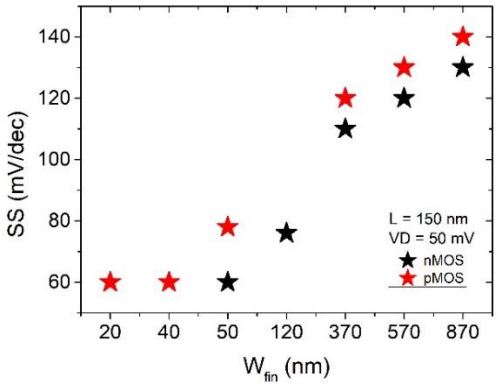
Figure 3. Threshold Voltage Measurements at (A) VDS= 50 mV and (B) 700 mV.

Figure 3 shows the obtained threshold voltage (V_{Th}) values as a function of the fin width, as well as for nMOS and pMOS, for drain voltage of 50 mV (A) and 700 mV (B). The threshold voltage degrades with the increase in fin width due to short-channel effects, which becomes more important as fin width becomes wider due to the lower electrostatic coupling. This behavior is even more pronounced at high drain voltage (figure 3B). However, in thinner fins, this effect is minimized, indicating that reducing the transistor's W_{Fin} makes it more robust to this variation and, therefore, it performs better in the saturation region as well.

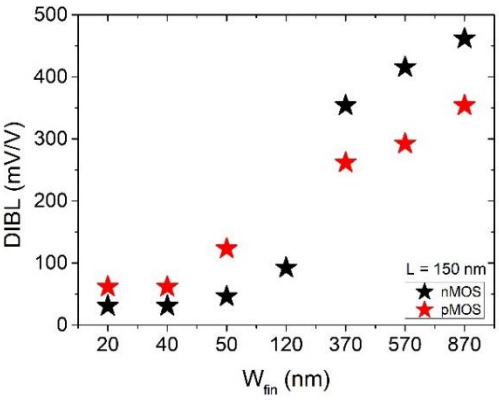
Figure 4 presents the subthreshold slope (A) and Drain Induced Barrier Lowering (DIBL) (B) as a function of fin width.

The subthreshold slope (SS), which indicates the switching speed of the transistor, is much higher in wider fins, a degradation caused by the less effective control of the drain current by the gate voltage. This also highlights the greater electrostatic coupling present in thinner fins, which better control the charges in the channel.

DIBL directly expresses how the drain voltage affects the device's threshold voltage. The DIBL can be calculated by $|V_{Th1}\text{-}V_{Th2}| / (V_{DS2} - V_{DS1})$, where V_{DS2} is 700 mV and V_{DS1} is 50 mV. The figure 4B shows a large degradation of DIBL with W_{fin} increase, showing how a strong short channel effect influence on wide transistors.



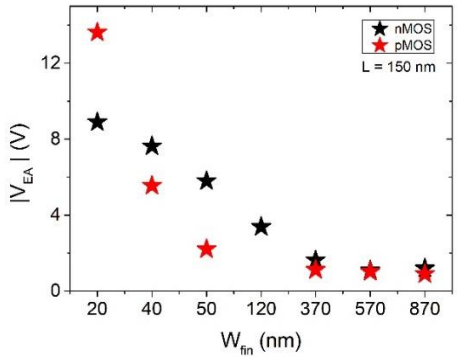
(A)



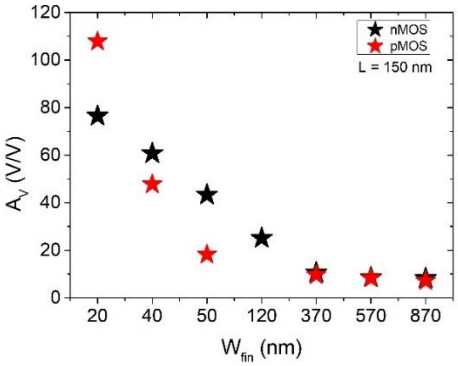
(B)

Figure 4. (A) Subthreshold Slope and (B) DIBL.

The Early voltage (V_{EA}) and the intrinsic voltage gain (A_V) are presented in figure 5, both are plotted as a function of fin width.



(A)



(B)

Figure 5. (A) Early Voltage and (B) Intrinsic Gain.

Analyzing the analog parameters, thinner fins also result in better analog behavior. The Early voltage shows a much higher value with smaller fin widths due to the reduced channel length modulation effect.

The intrinsic gain was proportional to the electrostatic coupling, showing a lower value for wider fins, where the gate's control over the channel charges is less effective. This behavior can also be explained by the higher electrostatic coupling and small effect of channel length modulation, which improves the Early voltage (which decreases with W_{Fin}) and consequently the intrinsic voltage gain.

Based on the better performance of SOI FinFETs with W_{fin}=20nm, this device was chosen to be applied in a basic analog circuit. In order to simulate this circuit nFinFET and pFinFET transistors were modeled in HSpice software based on its experimental behavior.

By utilizing the BSIM-CMG 106.1.0 model, a transistor with the selected dimensions was simulated. Parameters such as mobility and work function were adjusted to ensure the closest possible match between the experimental and simulated curves, as illustrated in Figure 6.

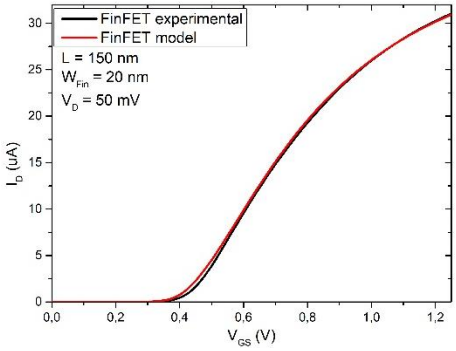


Figure 6. Comparison between model and experimental curve.

After calibrating the FinFET transistor, a two-stage operational transconductance amplifier was simulated using a power supply voltage of 2.1 V, to ensure approximately 0.7V drain voltage for each transistor, ensuring its operation. The differential pair of the transistor was designed to have a common mode voltage (V_{GS}) of 0.63V, which corresponds to a gm/I_D value of 8 V-1 (with 700mV of V_{DS}).

The bias current of the differential pair, with the design parameters, is 7.18µA per fin, and the other transistors were designed to meet this requirement by adjusting the number of fins for each transistor. The amplifier was initially designed to operate with the specifications presented in Figure 7.

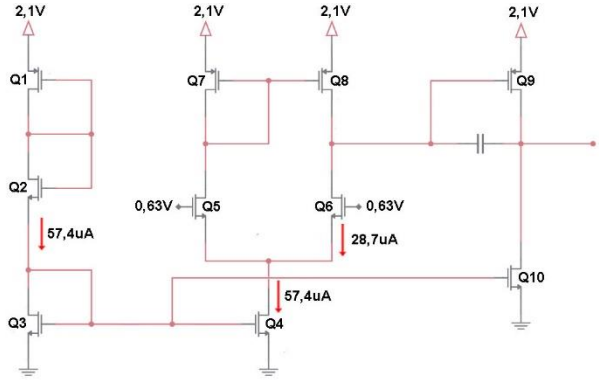


Figure 7. Two-stage amplifier design.

Various details such as the number of fins per transistor, expected voltages, currents, and types are provided in Table 2.

Table 2. Specifications of the simulated devices.

Transistor	Number of fins	Expected V_{DS} (mV)	Expected I_{DS} (µA)	Expected V_{GS} (mV)	Type
1	10	700	74,6	700	pmos
2	6	700	70,2	700	nmos
3	6	700	70,2	700	nmos
4	6	700	70,2	700	nmos
5 and 6	4	700	28,72	630	nmos
7 and 8	4	700	29,84	700	pmos

Figure 8A shows the voltage gain frequency response of proposed OTA, with a voltage gain reaching 68 dB and a gain bandwidth product (GBW) of 2.21 GHz. From figure 8B, it's

possible to observe a phase margin of 65.89º, both results shows that the triple gate FinFET can also be a good option to replace the planar devices in analog applications.

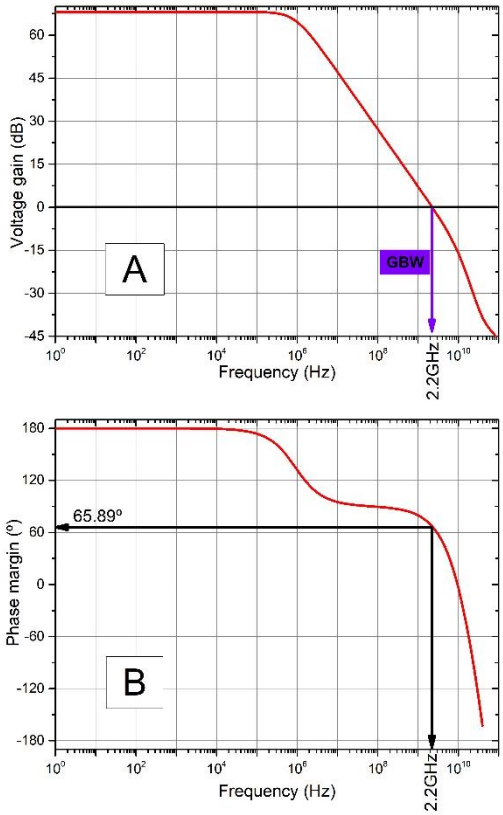


Figure 8. Amplifier voltage gain (A) and phase margin (B) as a function of frequency.

CONCLUSIONS

The first part of the research satisfactorily allowed us to investigate the behavior of the analyzed devices. After conducting the studies and analyzing the extracted parameters, it was possible to conclude that SOI FinFET, showed a significant improvement in all parameters with decreasing fin width (W_{Fin}) due to the greater electrostatic coupling i.e., increasing the gate's control capability over the channel.

The OTA circuit simulation achieved a high voltage gain and a wide frequency range, showing that FinFETs transistors also have good potential for application in analog circuits instead of just being used for digital applications.

ACKNOWLEDGMENT

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